

WHAT IS CLAIMED IS:

1. A method of reordering a scan chain for the design of testability on VLSI with low power dissipation, comprising the following steps of:

(a) inputting scan chain register circuit data, including the name of each register,

5 a 2D coordinates, and power dissipation value(s);

(b) inputting to test pattern data on the scan chain;

(c) inputting conditions of the design specification: (1) peak value of power dissipation at the time of potential conversion of register; (2) the maximum of total connection length of scan chain; and (3) the maximum of connection

10 distance between adjacent two registers;

(d) determining whether a Feasible Solution meeting the maximum limit of distance between two adjacent registers is provided;

(e) creating a database of the two adjacent registers;

(f) an event impossibility meeting both the maximum limited distance and the
15 maximum limited distance, and the total length of the scan chain being deleted;

(g) for the given test pattern, re-ordering the registers on the scan chain for reduction of power dissipation, and it being determined whether the peak value limit of power dissipation and the limit condition of maximum total
20 length for the scan chain connection accord; and

(h) outputting the updated scan chain arrangement and the corresponding scan chain test pattern data.

2. The method as claimed in claim 1, wherein steps of creating the database of the

two adjacent registers includes:

(a) dividing the distributed areas on the coordinates of all registers into the form of grids, and storing a grid attributed to each register;

(b) recording a register falling in each grid; and

5 (c) searching for a group of the two adjacent registers according to the maximum distance limit in the grid and in the circumference of the grid, and then recording them.

3. The method as claimed in claim 1, wherein an event impossibly meeting both the maximum limited distance is deleted in the case of

10 (a) existence in a register without any corresponding group of the two adjacent registers: indicating that the design is provided with no feasible solution;

(b) existence in a register with only an adjacent register: indicating that the register must be the output terminal of the scan chain, and its adjacent register is second in arrangement order;

15 (c) existence in two registers with only an adjacent register:

i. both of the two adjacent registers: indicating that no feasible solution is given; and

ii. two registers different from each other: indicating that one register can be made to be the input terminal of the scan chain, and the other, to be the output terminal; and

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(d) at least four registers with only an adjacent register: indicating that no feasible solution is given.

4. The method as claimed in claim 1, wherein an event impossibly meeting the

maximum of total connection length of scan chain is deleted in the case of

(a) $L_{lim} < L^{min}$: no feasible solution given;

(b) $L^{min} \leq L_{lim} < L^{max}$: at the time of the arrangement of the scan chain register at a next step, in addition to a search for a combination of the peak values in the adjacent registers so as to reduce power dissipation, a case beyond the total limit of length of the maximum scan chain also being taken into consideration so that the registers must be arranged to shorten the scan chain on the occasion; and

(c) $L_{lim} > L^{max}$: at the time of arrangement of the scan chain registers at a next step, the total limit of length of the maximum scan chain not being taken into consideration but a search for a set of peak values in the adjacent registers to reduce power dissipation; wherein i stands for any of the registers, and the distance D_i^{min} indicates the distance of a register i closer to the other registers, the distance D_i^{max} indicates the distance of a register i further from the other registers, and the distance D_i^{avg} indicates the distance of a register i equidistant from the other registers are estimated, namely $L^{min} = \sum_i D_i^{min}$, $L^{max} = \sum_i D_i^{max}$, and $L^{avg} = \sum_i D_i^{avg}$.

5. The method of reordering a scan chain for the design of testability on VLSI with low power dissipation as claimed in claim 1, wherein scan chain registers are reordered to

(a) decide a next optimal register to be arranged; and

(b) decide an optimal register of the output terminal.

6. The method of reordering a scan chain for the design of testability on VLSI with

low power dissipation as claimed in claim 5, wherein in order to decide a next optimal register to be arranged, the algorithm tool according to this invention uses a logical XOR calculation to every time sort out a next optimal register in a set of registers having not been arranged in the course of arrangement so that the opposite test patterns can be little different from the test patterns of registers so far having been arranged, thereby reducing the probability of register state conversion in each shift.

7. The method of reordering a scan chain for the design of testability on VLSI with low power dissipation as claimed in claim 3, wherein in order to decide an optimal register of the output terminal after the scan chain registers reordered includes:

(a) the special case of the built database of registers adjacent to each other occurs when (1) a register is existed with an adjacent register only; and (2) two registers are existed respectively with an adjacent register only, and the two registers are different from their adjacent registers;

(b) when no special cases occur, the minority of adjacent registers among all registers is used as the registers at the output; and

(c) when a database of registers adjacent to each other is provided, of all registers, a register of maximum power dissipation is used as an output terminal, and that less different from the test pattern is used as an input terminal.